HP83000 Model F660 Specifications

Channel Specifications Driver		
pulse performance at pin, measured into 50 0hms at coaxial connector:		
at level	ECL (-1.7V, -0.9V)	CMOS (0.5V, 3.5V)
transition times (20% to 80%) (typ.)	<250ps	<350ps
min. pulse width	0.75ns	1ns
typical	0.6ns	
source impedance	50ohms±5%	
max. output current	>50mA	
output swing[1]	0.5V to 5V into open	
level range (low level/high level)	-2.5V to +3V / -1.5V to +5.5V	
level resolution	10mV	
level accuracy (DC)	+(2OmV + 0.1% of programmed level)	
high-Z compliance levels (I/O pins)	Vlow to (Vhigh + 500mV)	
data formats	600MHz mode	330MHz mode
inputs (I) mode	DNRZ + High Z	DNRZ +High Z
	RZ+HighZ	RZ+HighZ
	R1+HighZ	R1+HighZ
	RC+HighZ	RC+HighZ
bidirectional (I/O) mode	-	DNRZ ± High Z
Channel Specifications Comparator		
threshold range (single threshold, prog. per pin)	-2.5V to 5.5V	
threshold resolution	10mV	
threshold accuracy	± (20mV + 0.1% of programmed value)	
min. detectable pulse width	300ps	
min. overdrive	10% of programmed amplitude, min. 150mV	
impedance		
terminated by corresponding driver	50 ohms($\lvert r\rvert \leq$ 10% at $t_r \geq$ 250ps)[2]	
high-Z	10κΩ parallel with 15pF (lumped)	
compare modes	660MHz mode	330MHz mode
output (O) mode	edge, window	edge, window
bidirectional (I/O) mode	-	edge

[1] programmable down to 0V.

[2] Where: r = reflection coefficient
t_r = rise time

Timing Specifications

timing measurement accuracy[3]	
edge placement accuracy[4] :	± 50ps
Driver	± 80ps
Receiver	± 80ps
edge placement resolution	10ps
edge placement range:	
driver leading edge (DLE)	-4 to +12 periods, (within –100ns to + 500ns)
driver trailing (DTE)	DLE +0.50ns to DLE + period -0.50ns, (within -100ns to +500ns)
comparator leading edge (CLE)	-4 to +12 periods, (within –100ns to +500ns)
comparator trailing edge (CTE)	CLE +0.75ns to CLE + period -0.75ns, (within –100ns to +500ns)
high-Z to active edge placement accuracy	1ns
vector period	660MHz mode 330Mhz mode
range	1.50ns to 500ns 3.00ns to 500ns
accuracy	± 0.1% of period
resolution	3 digits
external clock	
period range	750ps to 500ps
synchronization	period = n*external clock period (n = 1,2,4,8)

DC Parametric Measurement Unit Specifications

1 PMU per I/O board (16 channels), switchable to each channel within one I/O board.

operating modes: — measure voltage — force voltage / measure current
— measure current — force current / measure voltage

Mode	Range	Resolution	Accuracy[5]
voltage force	± 10V	5 mV ±0.5%	±20mV-(Ia* R)
	±2V	1 mV	±0.5% ±4mV-(Ia*R)
voltage measure	±10 V	5 mV	±0.3% ±10mV-(Ia*R)
	±2V	1 mV	±0.3% ±3mV-(Ia*R)
currentforce	±200mA	100µA	±0.5% ±1mA
	±20mA	10µA	±0.5% ±100µA
	±2mA	1µA	±0.5% ±10µA
	±200µA	100nA	±0.5% ±1µA
	±20µA	l0nA	±0.5% ±l00nA
	±2µA	1nA	±0.5% ±20nA
current measure	± 200mA	100µA	±0.5% ± 1 mA
	±20mA	10µA	±0.5% ±100µA
	±2mA	1mA	±0.5% ±10µA
	±200µA	100nA	±0.5% ±1µA
	±20µA	l0nA	±0.5% ±100nA
	±2µA	1nA	±0.5% ±20nA

[3]For setup, hold and propagation-delay measurements after reference measurement. Timing formats for pin under test must be DNRZ/Edge Compare. Timing can be varied for one pin at a time at stable settings and temperature.

[4]Valid for all pins at all settings and conditions at all calibrated frequencies and levels.

[5]Accuracy specifications are given as % of programmed or measured value
Ia = actual current. R = wiring resistance; (see DUT interface types).